CLAIMS

What is claimed is:

1) (original) A method comprising:

forming a sacrificial gate electrode on a substrate;

forming sidewall spacers on the sides of the sacrificial gate electrode forming a sacrificial inter-level dielectric layer;

removing the sacrificial gate electrode;

depositing a replacement gate electrode;

polishing the sacrificial inter-level dielectric layer and the replacement gate electrode; and

performing a wet etch removal on the inter-level dielectric layer and any residual gate electrode material not in the gate trench.

2) (original) The method of claim 1 wherein the sidewall spacers are silicon nitride or carbon doped nitride.

3) (original) The method of claim 1 wherein the sacrificial inter-level dielectric layer is a soft chemical vapor deposition oxide or a stoichiometric silicon nitride.

4) (original) The method of claim 1 wherein polishing the sacrificial inter-level dielectric layer and the replacement gate electrode removes less than 50 Angstroms of the replacement gate height.

5) (original) The method of claim 1 wherein performing the wet etch removal removes remaining defects from the polishing the sacrificial inter-level dielectric layer and the replacement gate electrode.

6) (original) The method of claim 5 wherein the wet etch removal is performed using phosphoric acid, conditioned phosphoric acid, aqueous hydrofluoric acid, a buffered hydrofluoric acid solution, or a hydrofluoric acid used with surfactants.

7) (original) The method of claim 6 wherein the surfactant used with the hydrofluoric acid is ethylene glycol.

8) (original) The method of claim 5 wherein the wet etch removal process is performed at a temperature of approximately 20 degrees Celsius to about 30 degrees Celsius.

9) (original) The method of claim 5 wherein the wet etch removal process persists for a time period of approximately 2 minutes to 5 minutes.

10) (original) The method of claim 5 wherein the wet etch removal process has an approximate selectivity of 10:1 or greater.

11) (original) The method of claim 1 wherein the wet etch removal removes under 10 Angstroms of height from the replacement gate electrode.

12) (original) The method of claim 1 wherein performing the wet etch removal process of the residual gate electrode material comprises using a titanium nitride etch in a sulfuric acid and hydrogen peroxide mixture, at 70 degrees Centigrade.

13) (original) The method of claim 12 wherein the titanium nitride etch removes the inter-level dielectric layer at a rate of approximately 60 Angstroms per minute.

14) (original) The method of claim 1 further comprising depositing a nitride etch stop layer.

15) (original) The method of claim 14 wherein the nitride etch stop layer creates stress in an underlying structure.

16) (original) The method of claim 1 further comprising depositing a nitride etch stop layer creating stress in an underlying structure.

17) (original) A method comprising:

forming a sacrificial gate electrode on a substrate;

forming sidewall spacers on the sides of the sacrificial gate electrode forming a sacrificial inter-level dielectric layer;

removing the sacrificial gate electrode;

depositing a replacement gate electrode;

polishing the sacrificial inter-level dielectric layer and the replacement gate electrode; and

performing a wet etch removal on the inter-level dielectric layer and the gate electrode; and

depositing a nitride etch stop layer creating stress in the underlying structure.

18) (original) The method of claim 17 wherein the deposition of the nitride etch stop layer is formed as a blanket deposition over an entire substrate.

19) (original) The method of claim 17 wherein the deposition of the nitride etch stop layer is selectively formed over individual devices or transistors.

20) (original) The method of claim 17 wherein the deposition of the nitride etch stop layer is performed using a chemical vapor deposition process using silane and nitrogen or ammonia.

21) (original) The method of claim 17 wherein the nitride etch stop layer consists of a silicon nitride (Si3N4).

22) (original) The method of claim 17 wherein the nitride etch stop layer is from the group consisting of germanium, silicon germanium, carbon-doped silicon oxide, and

carbon-doped silicon nitride.

23) (original) The method of claim 17 wherein the deposition of the nitride etch stop layer is between 100 to 1200 Angstroms thick.

24) (original) The method of claim 17 wherein the deposition of the nitride etch stop layer is approximately 500 Angstroms thick.

25) (original) The method of claim 17 wherein the nitride etch stop layer deposition is formed at temperatures close to or less than 400 degrees Centigrade for less than 1 minute.

26) (original) The method of claim 25 wherein the nitride etch-stop layer is compatible with temperature sensitive metal gate electrode candidates.

27) (original) The method of claim 17 wherein an inter level dielectric layer is deposited after the nitride etch stop layer has been deposited.

28) (original) A transistor formed on a substrate comprising:

a metal gate electrode;

sidewall spacers formed on the sides of the gate electrode;

a nitride etch stop layer deposited over the gate electrode and sidewall spacers, that creates stress in the underlying transistor structure; and

an inter-level dielectric layer formed over the sidewall spacers, the gate electrode, and nitride etch

stop layer.

29) (original) The method of claim 28 wherein the metal gate comprises material or materials from the group consisting of aluminum (Al), titanium (Ti), molybdenum (Mo), tungsten (W), titanium (TiN, TiC) and tantalum (TaN, TaC).

30) (original) The method of claim 28 wherein the replacement gate material is composed of multiple metals.